EE 505

Lecture 15

String DACs

Current Steering DACs

General Performance Concerns:

1. Glitch
2. Ringing
3. Incomplete Settling
4. Kickback
    1. Output feeding back to the input due to gate to drain capacitance
5. Mismatch
    1. Local Random Variations (Handled with area)
    2. Gradient Effects (Handled with Common Centroid)

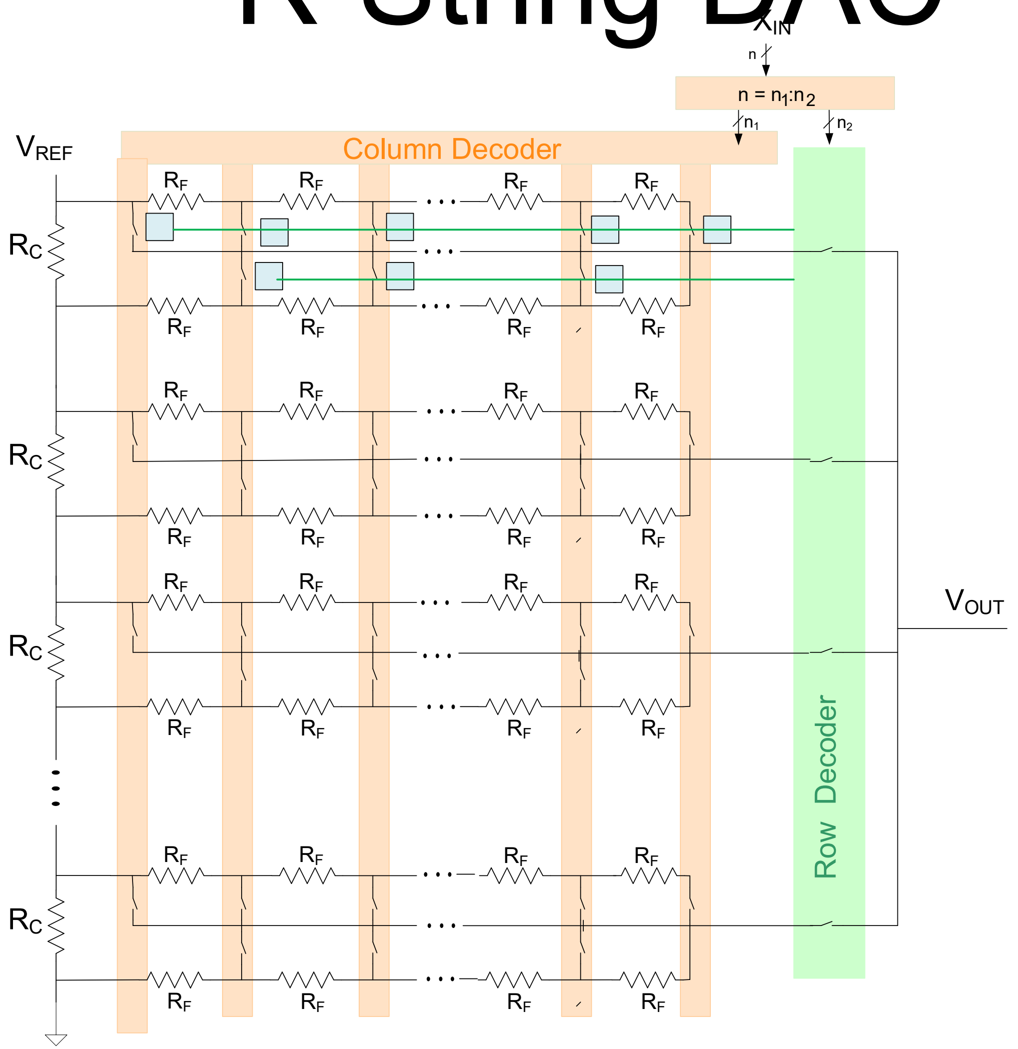
String DACs:

1. Large number of elements
2. Routing is significant for decoder
    1. Matrix Decoder dramatically simplifies routing
        1. Severe previous code dependance (Can have memory)
    2. Tree Decoder with Pass Transistor Logic can help as well
    3. Row and Column Decoder can be used to decrease area
    4. Fine String Interpolator
        1. Reduces decoder complexity
        2. Reduces number of switches and resistors
        3. Could use 2 interpolators for when interpolator is near VDD or near 0
        4. Switch resistance determines tap voltages
3. Fairly Large INL
4. Significant Previous Code Dependance (Large Parasitic Capacitance)
5. Gradient Effects can cause trouble (Common Centroid Difficult)
    1. Include a course string to dump most of the area into for common centroid layout
6. Settling time dependant on Thevenin impedance

Current Steering DACs:

Review from Last Lecture

R-String DAC



Note Dual Ladder is used !

: AND pixel sensor gate

32x32 Matrix

A 10-b 50-MHz **CMOS D/A** converter with 75-ω buffer

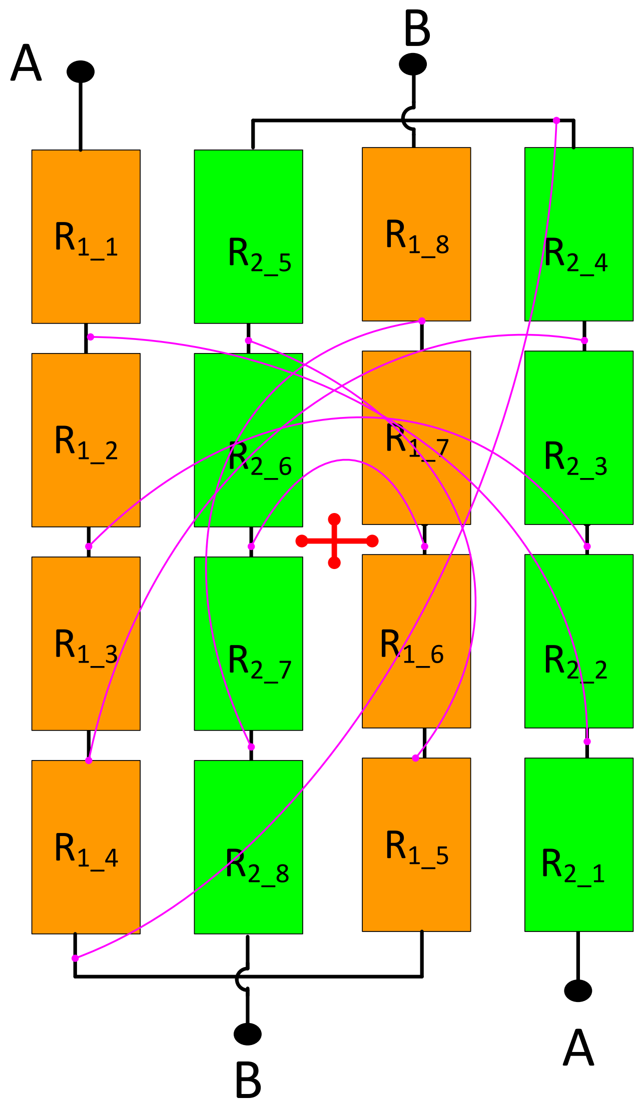
MJM **Pelgrom** - Solid-State Circuits, IEEE Journal of, 1990 - ieeexplore.ieee.org

Abstracf-A 10-b 50-MHz digital-to-analog (D/A) converter is pre-sented which is based on a dual-ladder resistor string. This approach allows the linearity requirements to be met without the need for selection or trimming. The D/A decoding scheme reduces the glitch energy, ...

Cited by 109 Related articles All 3 versions Cite Save

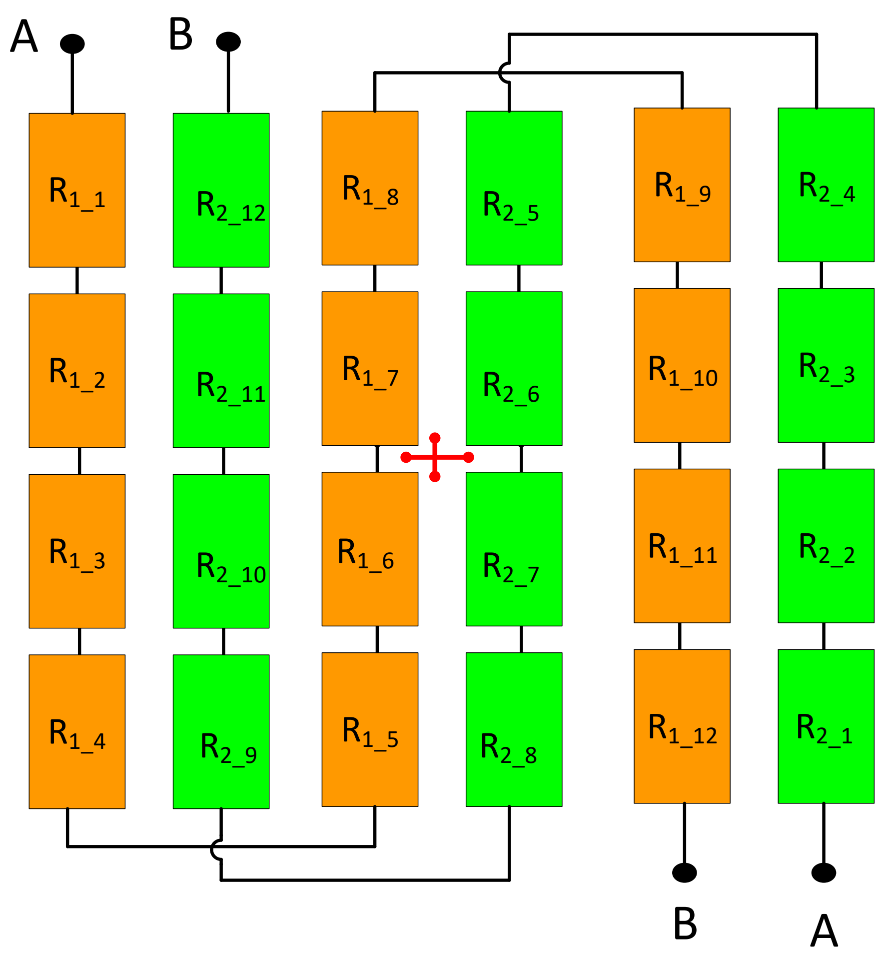
Review from Last Lecture

Common-Centroid Anti-Parallel Ladder Layout



Review from Last Lecture

Common-Centroid Anti-Parallel Ladder Layout

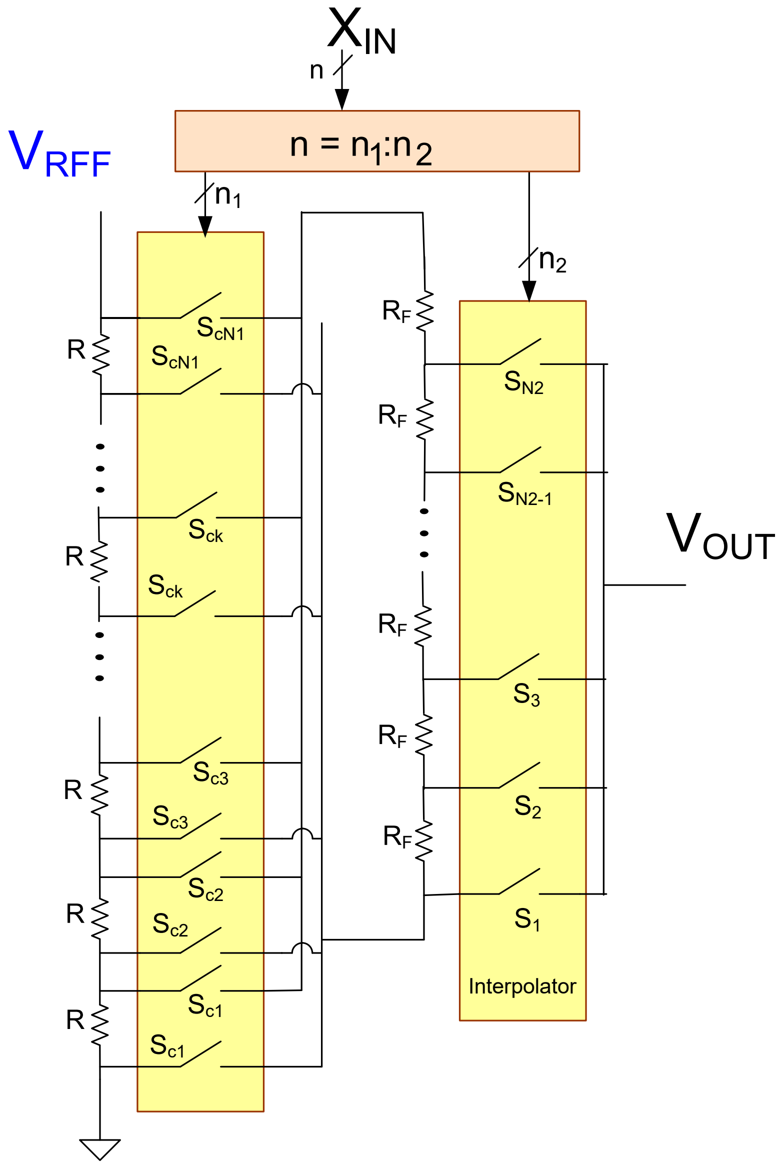


Interconnects Not Shown

Review from Last Lecture

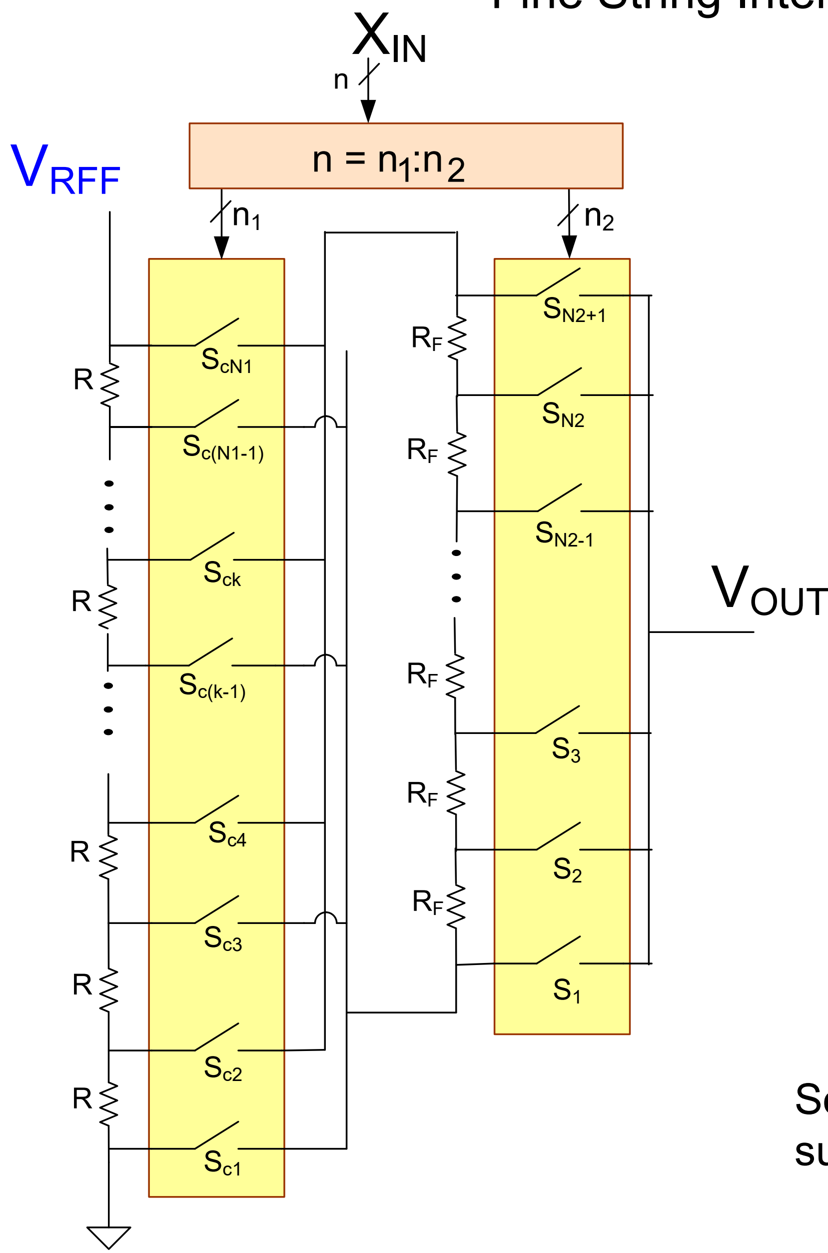
R-String DAC

Fine String Interpolator



R-String DAC

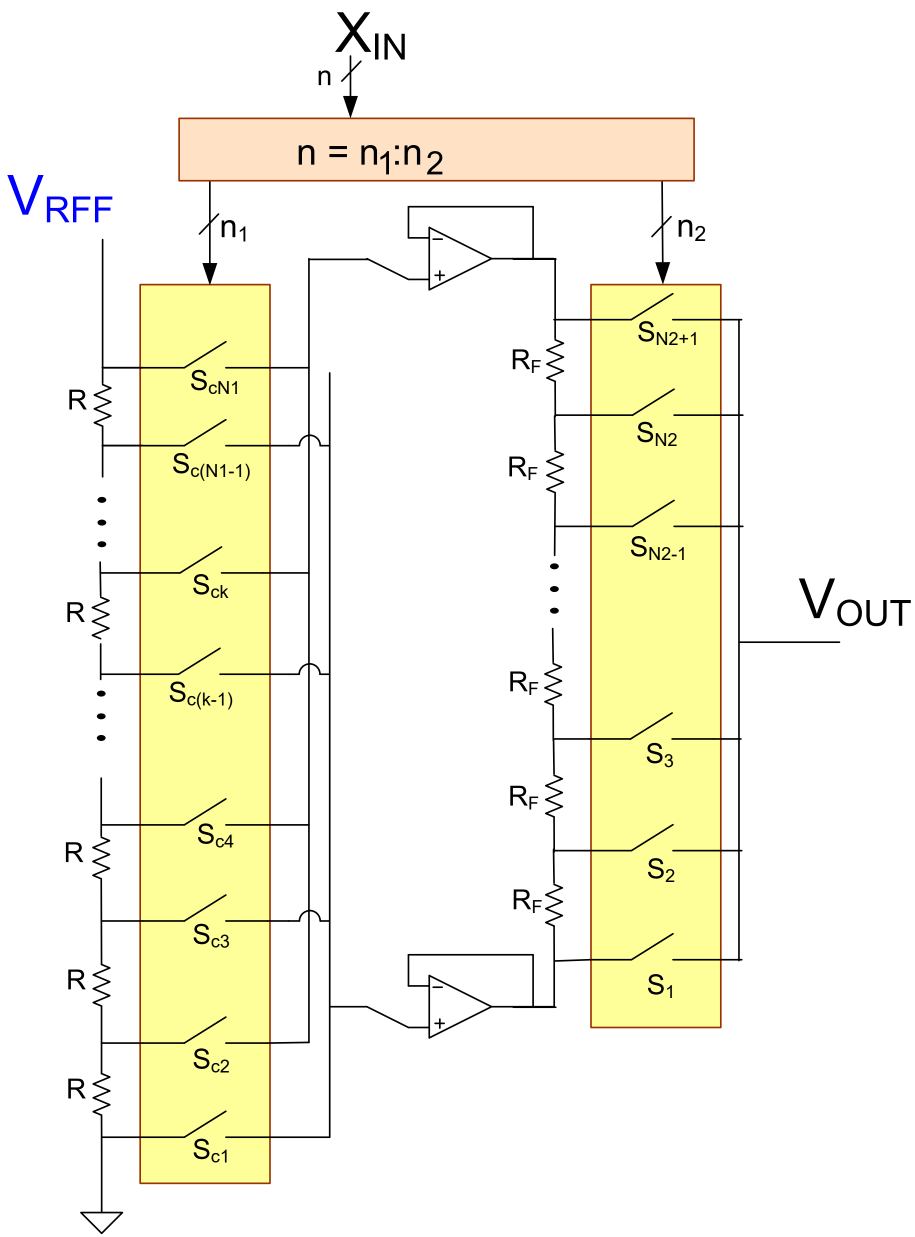
Fine String Interpolator



Sometimes termed sub-divider, sub-range or dual-string DAC

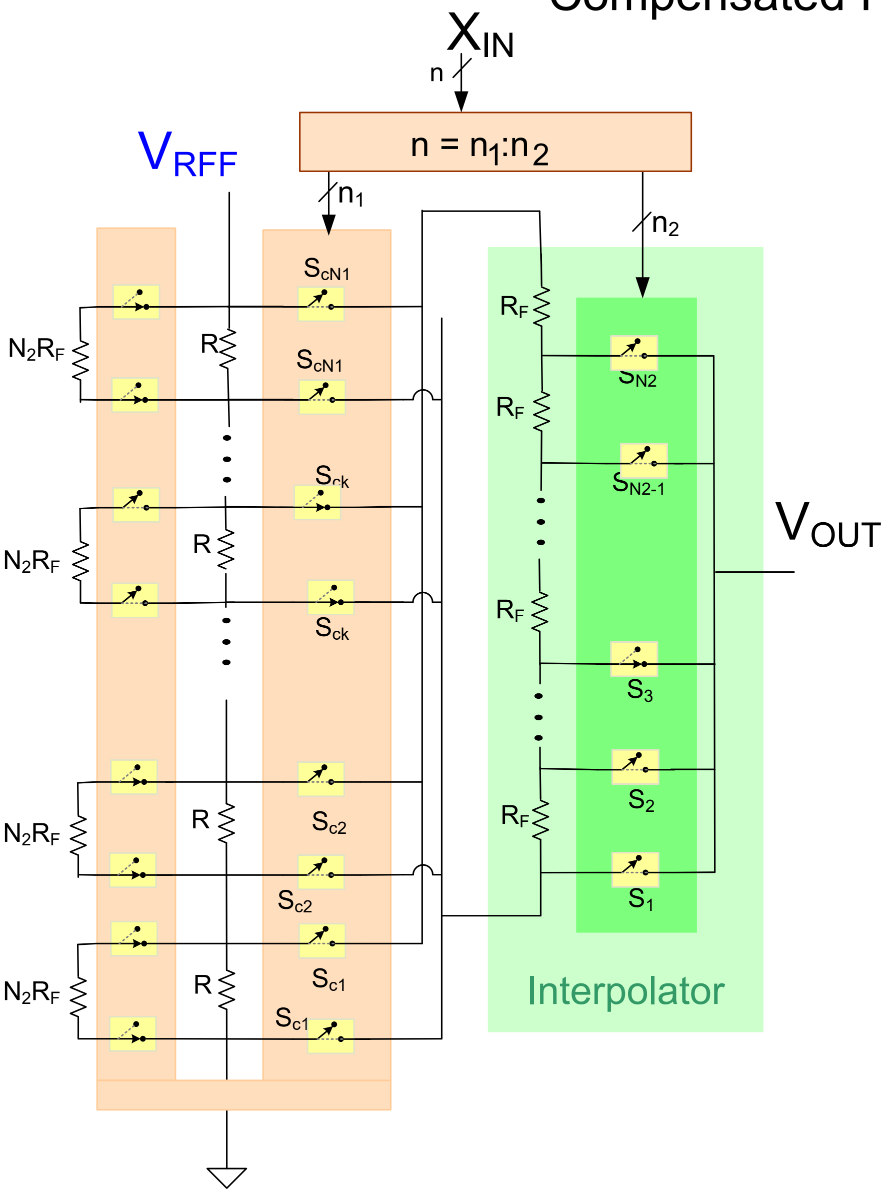
R-String DAC

Buffered Fine String Interpolator



R-String DAC

Compensated Fine String Interpolator



$$N_2 = 2^{n_2}$$

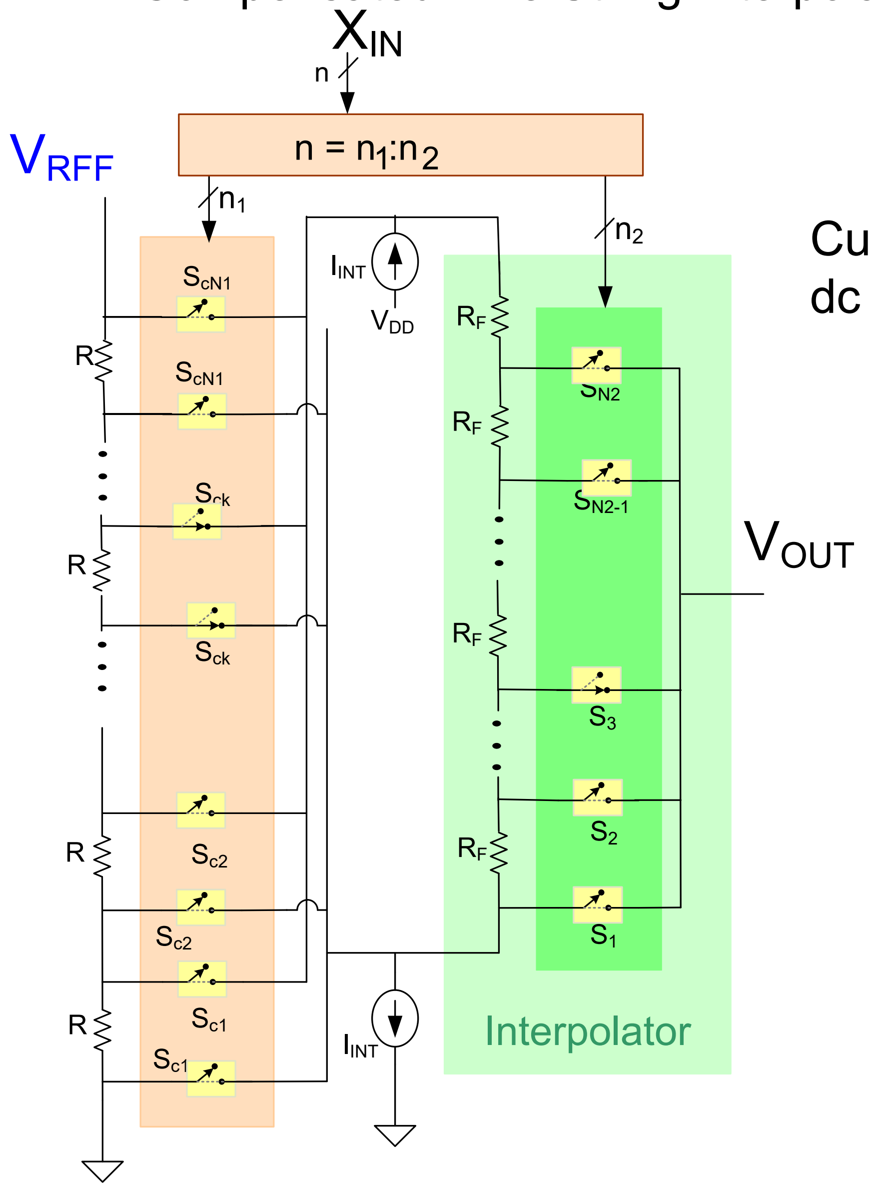
Paralleling each R will be either the interpolator or a resistor of value N_2R_F

Area of N_2R_F resistors may be very small

Tap voltages on coarse R-string should not change with X_{IN}

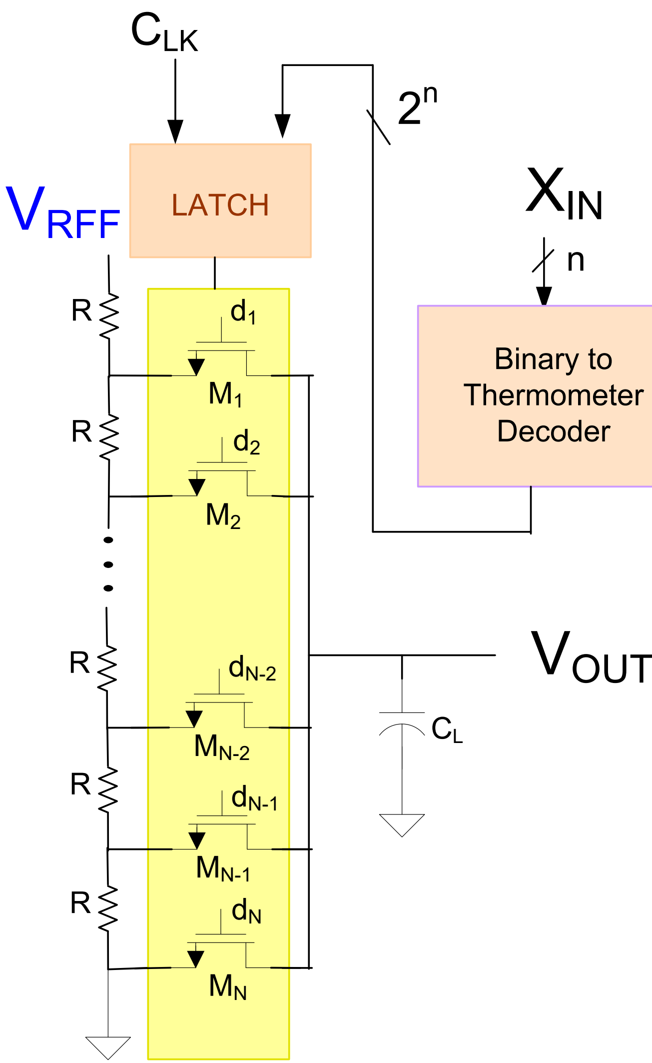
R-String DAC

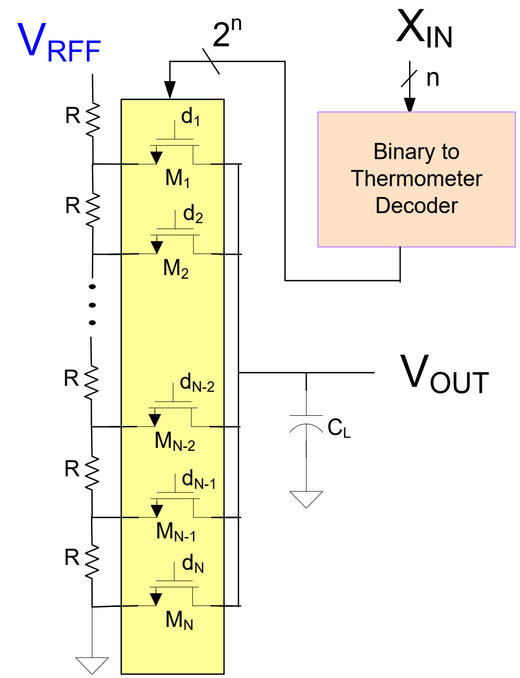
Compensated Fine String Interpolator

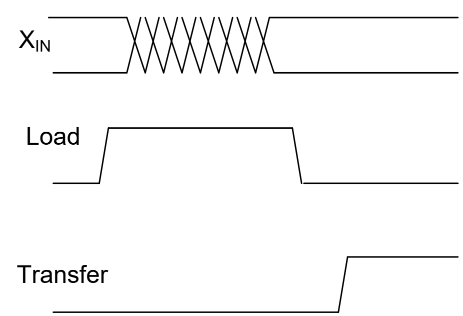


Current Sources have same dc current as interpolator

Basic R-String DAC



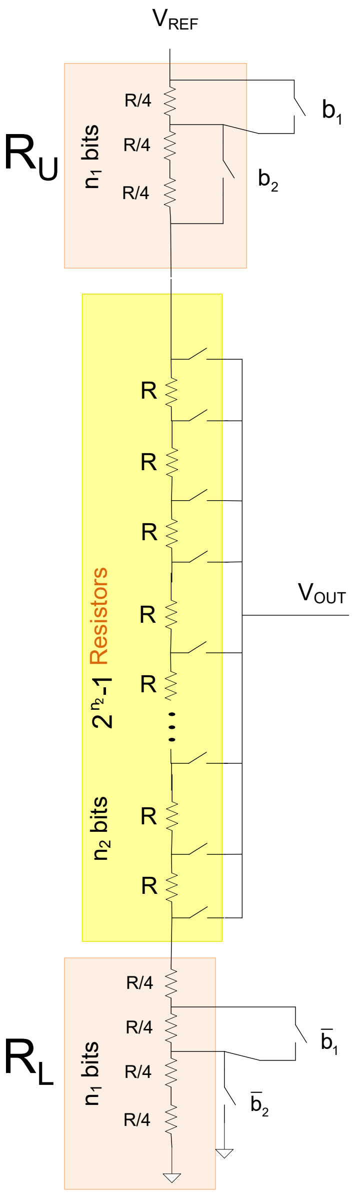




Latching Boolean Signal Can Reduce/Eliminate Logic Transients which Cause Distortion

Basic R-String DAC

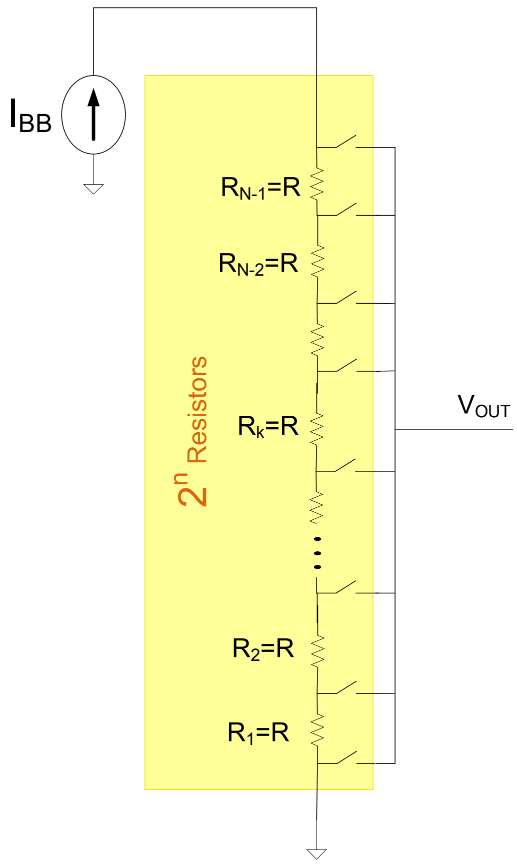
Dither DAC

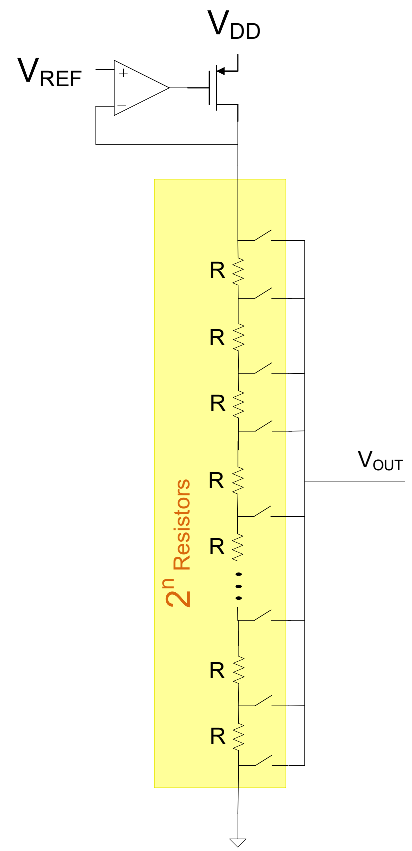


For all b_1 and b_2, $R_U+R_L=R$

- Another Segmented DAC structure
- Can be viewed as a “dither” DAC
- Often n_1 is smaller than n_2
- Dither can be used in other applications as well

Basic R-String DAC





$$V_{0k}=I_{BB}\bullet\sum_{i=1}^{k}R_k \qquad \text{for } k\geq 1$$

Impedance facing V_{OUT} is code dependent

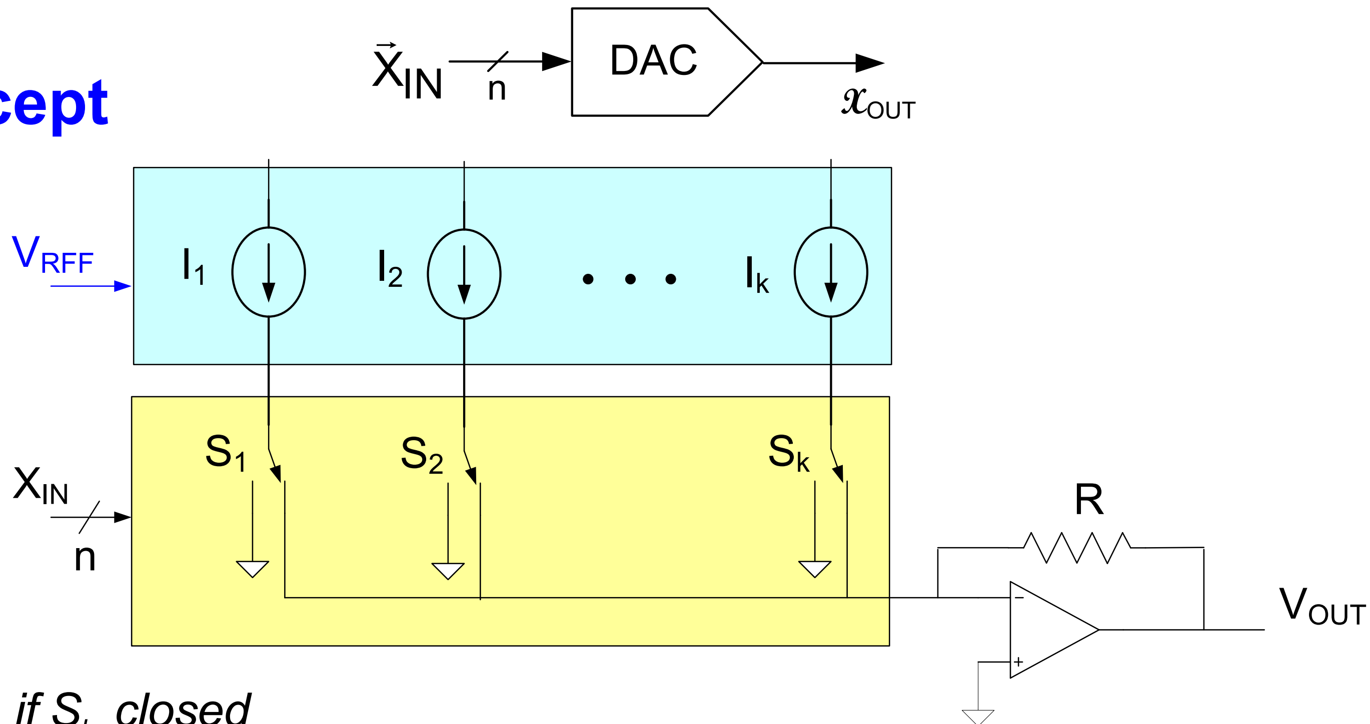
No loading of V_{REF}

Kickback to V_{REF} removed

Current Steering DACs

Current Steering DACs

Concept



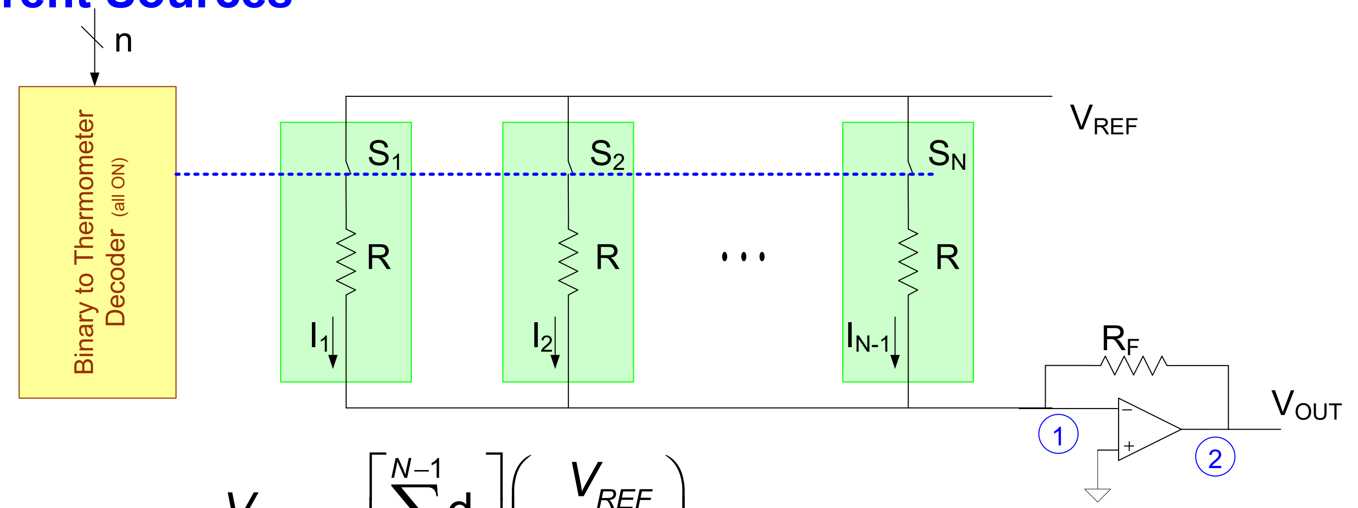
$$d_k = \begin{cases} 1 & \text{if } S_k \text{ closed} \\ 0 & \text{if } S_k \text{ open} \end{cases}$$

$$V_{OUT} = \left[\sum_{l=1}^{k} d_i I_i \right] (-R)$$

- Current sources usually unary or binary-bundled unary
- Termed bottom-plate switching
- Can eliminate resistors from DAC core
- Op Amp and resistor R can be external
- Can use all same type of switches
- Switch impedance not critical nor is switch matching
- Popular MDAC approach

Current Steering DACs

Unary Current Sources



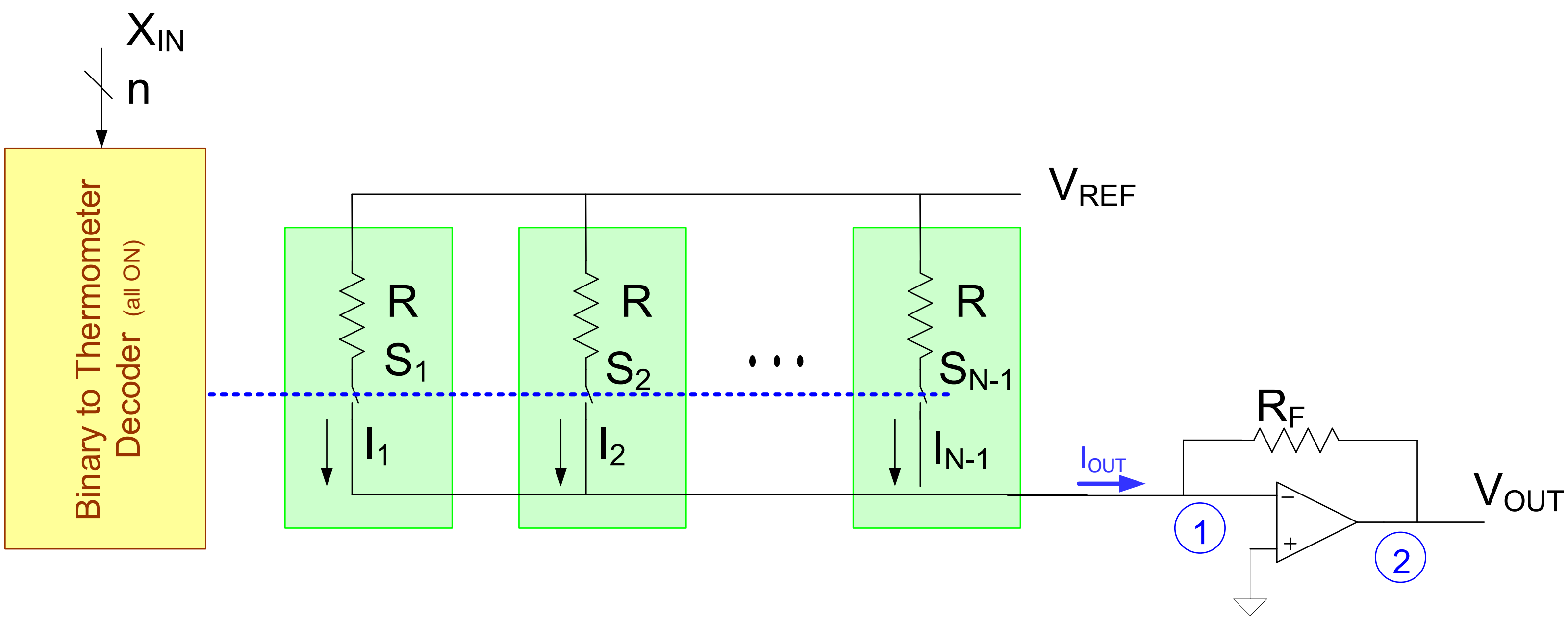
$$V_{OUT} = \left[\sum_{I=1}^{N-1} d_i\right]\left(-\frac{V_{REF}}{R}\right)$$

Inherently Insensitive to Nonlinearities in Switches and Resistors

- Termed “top plate switching”
- Thermometer coding (routing challenge!)
- Excellent DNL properties
- INL may be poor, typically near mid range
- Switch kickback to V_{REF}
- Not suitable for use as MDAC

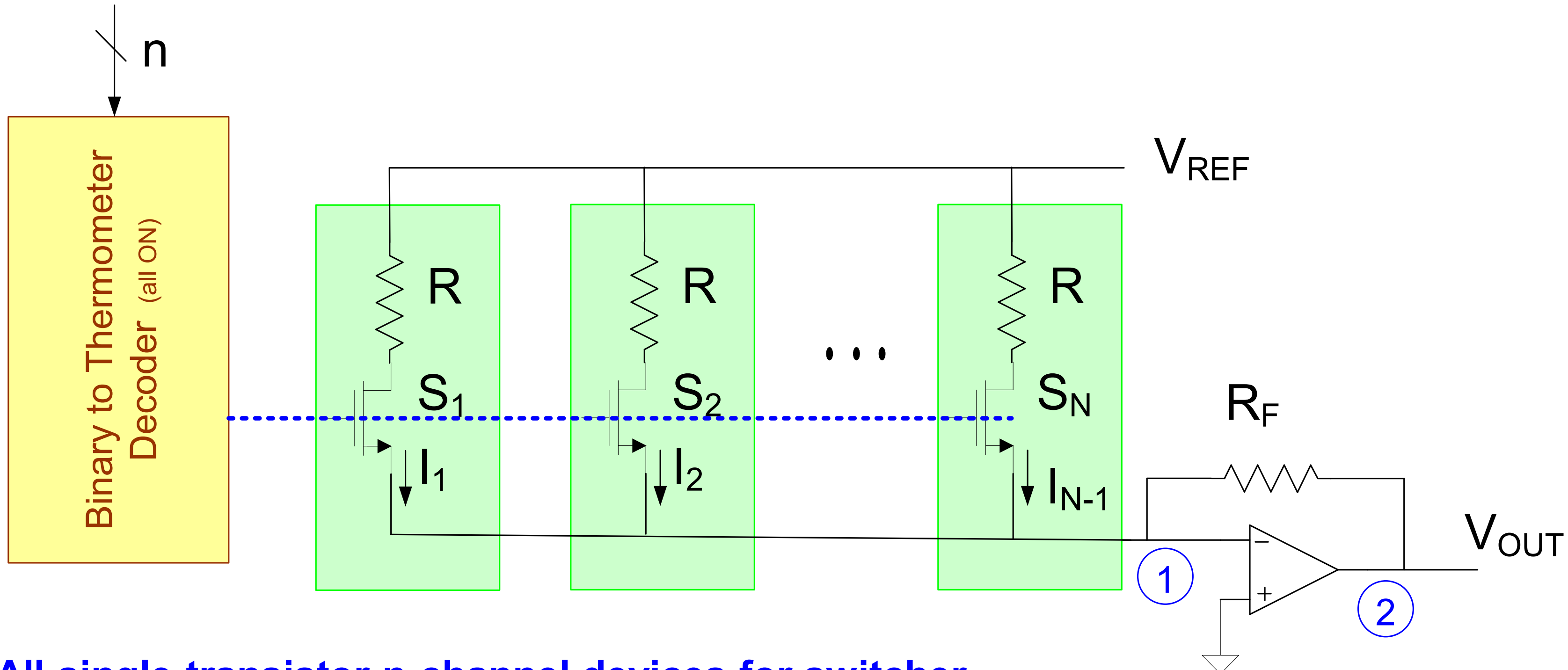
Current Steering DACs

Unary Current Sources



- **Inherently Insensitive to Nonlinearities in Switches and Resistors**
- **Smaller ON resistance and less phase-shift from clock edges**
    - Termed “bottom plate switching”
    - Thermometer coded
    - Can be used as MDAC
    - Reduced kickback to V_{REF}

Current Steering DACs



- **All single-transistor n-channel devices for switcher**
- **Unary R:switch cells**
- **Parasitic capacitances on drain nodes of switches cause transient settling delays**
- **R+Rsw is nonlinear (so nonlinear relationship between I_k and V_{REF}) but does not affect linearity of DAC**
- **Resistor and switch impedance matching important**
- **Previous code dependent transient** (parasitic capacitances on drains of switches)

Stay Safe and Stay Healthy !

End of Lecture 15